Claims 1-16 were rejected under 35 USC §103(a) as being unpatentable over the Applicants Admitted Prior Art (AAPA) in view of Hoskins (U.S. Patent No. 5,872,978). Applicants respectfully traverse this rejection and submit that claims 1-16 recite subject matter not shown or suggested by any combination of the cited prior art.

Claim 1 defines a method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo-instruction and at least one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction (collectively, instruction). The pseudo-instruction is arranged before the at least one instruction and indicates that at least one instruction or data follows the pseudo-instruction. At least one instruction address or data address is part of the pseudo-instruction. The method includes steps of reading the program from the memory, detecting the pseudo-instruction, prefetching the instruction or data from the memory in accordance with the at least one instruction address or the data address, and storing the prefetched instruction or data in a buffer.

As a result of the claimed configuration, a method is provided for prefetching instructions and data of a program stored in a memory. The method includes prefetching an instruction or data from a memory in accordance with at least one instruction address or data address and storing the prefetched instruction or data in a buffer. The instruction address or data address is the part of a pseudo-instruction that is arranged before a predetermined instruction. The instruction address indicates the jump destination of the predetermined instruction, and the data address indicates the address of the data that is necessary for the predetermined instruction. By using the pseudo-instruction and the instruction address or data address, the predetermined

instruction can be acquired from the buffer without error. The instruction is prefetched from the memory and is stored in the buffer before the instruction is executed. When it is determined that the instruction should be executed, the instruction is already stored in the buffer. Therefore, it is possible to continuously execute branch instructions without encountering a mis-hit.

Hoskins is directed to an apparatus for translation of program data into machine code format. The apparatus includes an encoder compiler (18) that generates and inserts in a common format code stream a number of pseudo-instructions. Hoskins describes that the pseudo-instructions provide guidance to a decoder translator (24) aimed at improving the speed of economy of translation to the native code. In other words, the pseudo-instructions are used to efficiently perform translation of the program data. For example, the pseudo-instruction BRANCH_LIKELY inserts the translator (24) that a conditional branch instruction follows the pseudo-instruction. See col. 4, lines 38-41. The translator (24) translates the branch instruction in accordance with the pseudo-instruction. Hoskins does not show or suggest that an instruction follows a pseudo-instruction that includes the instruction address or the data address, as defined by the claimed invention. Since Hoskins does not teach or suggest prefetching an instruction using the pseudo-instruction that includes the instruction address or the data address, Hoskins cannot continuously execute the branch instructions to improve the processing efficiency, as defined by the claimed invention.

Applicants submit that AAPA does not teach or suggest using the pseudo-instruction that includes the instruction address or the data address. Page 2, lines 8-19 of the present specification clearly describes that a circuit for generating the branch

destination address of the branch instruction is necessary. Accordingly, the APPA does not use the pseudo-instruction including the instruction address or the data address. Thus, no combination of Hoskins and AAPA can achieve the present invention, as defined by claim 1, upon which claims 2-15 depend. Furthermore, Applicants submit that there would be no motivation to combine the references as suggested by the Office Action. Accordingly, Applicants request that the rejection be withdrawn and that claims 1-16 be allowed.

Claims 17-18 were objected to for relying on a rejected base claim, but would be allowed if rewritten into independent form. Since the rejections of the base claims have been completely addressed herein, Applicants submit that claims 17-18 are in condition for allowance.

In view of the above remarks, the Applicants respectfully submit that each of claims 1-18 recite subject matter which is neither disclosed nor suggested in the cited prior art. Applicants submit that this subject matter is more than sufficient to render the claimed invention unobvious to a person of ordinary skill in the art. Applicants therefore request that each of claims 1-18 be found allowable, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not timely filed, the Applicants respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,

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